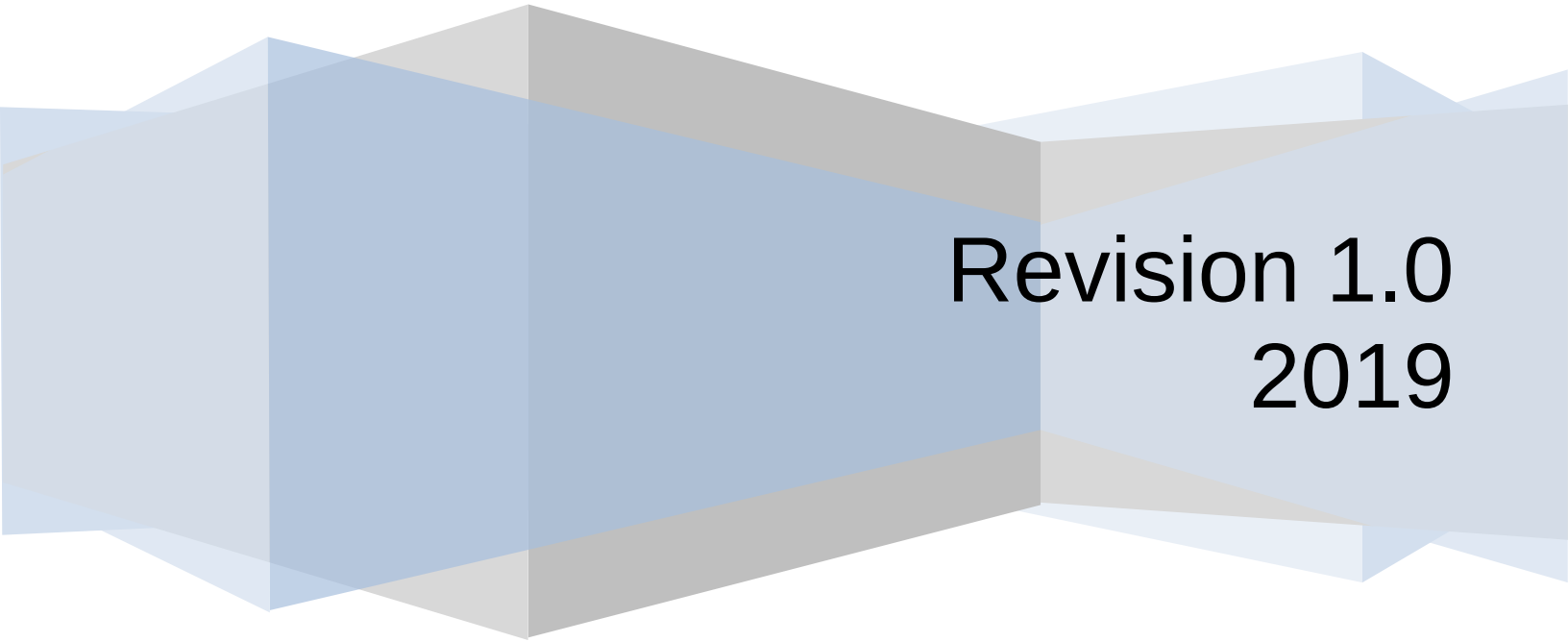
Acculogic Inc.

DFT - Simplified

Ten Design for Testability rules for a successful design



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1. Provision of tooling holes

In order that the connections can be made to the board, it is necessary to have accurate position or location holes that can be used to accurately locate the PCB onto the test fixture. In this way the PCB can make accurate location onto any probes or connections required. Requirements for the tooling holes may include:

* Three preferred but a minimum of two, on opposite diagonal corners
* Tooling or location holes should not be plated to ensure their accuracy
* Tooling or location holes should not be obscured, and they should be free from components etc. in the vicinity of the hole to enable any locating spigots on the test fixture to mate with the hole.
* Location accuracy of the tooling or location holes should typically be within 0.05 mm, i.e. 0.002 inches, although with techniques changing all the time, check the requirements for the actual tester.

2. Provide a probe-able pad for each circuit net

When using in-circuit testing, it is necessary to get access to each net in the circuit to enable enough test coverage to be achieved. Probe-able test pads are ideally dedicated test pads, but with circuits becoming much smaller this is not always possible. There are alternative techniques to test DUT without applying direct test pad, such as boundary scan and silicon nails technique.

3. Probe-able test pads should all be on one side of the board

When possible test pads for the test probes should all be on the same side (underside) of the PCB. This means that single sided fixtures can be employed. These are cheaper, simpler and faster to use than double sided fixtures. However double-sided probing is possible.

4. Provision of even distribution of test points across the board

The test pins must not exert a force greater than 96 oz over any square inch of board area (the force is equivalent to a maximum of twelve 8-oz test pins over any square inch of PCB). A localized area of high force may cause the PCB to flex, possibly fracturing solder joints and damaging internal trace layers.
Place test points around the perimeter of BGA's. This will help reduce the stress on the BGA solder joints. Special consideration can be given to areas of high probe density by providing clearance area on the opposite of the PCB to allow placing of push-fingers to counter the probe force and minimize the board flexing.

5. Test target diameter

The recommended test point size is 30mils or larger. If **30 mil** test points are not feasible, the size may be reduced to as low as 24 mils. Special fixturing considerations such as guided probe fixturing technology must be used to accurately probe the sub **30 mil** test points. Furthermore, accurate tooling hole diameter (see tooling hole section) and solder mask clearance must be considered. The solder mask clearance should be within 3 mils. Smaller test points would increase the possibility of probes missing the test point targets, resulting in an unreliable test or an untestable component. Unreliable contacts will lead to board re-test and eventually to an increased test cost.

6. Test-point clearance to the edge of panel/Board

Test-point centers must be **.125"** from the edge of the PCB.

7. Test-point center to center spacing clearance

There are 4 types of probes that are commonly used in the ICT industry. They are known as **100 mil, 75mil, 50 mil and 39 mil** probes. The **100 mil** and **75mil** probes are the most reliable and are also low cost. The **50 mil** probes are less reliable and higher cost. It is recommended to use as few **50 mil** probes as possible. The **39 mil** probes are very fragile and are also very expensive. They must be used only if there are no alternatives.
> **100 mil** probe center to center spacing requirement: **85 mils**
> **75 mil** probes center to center spacing requirement: **70 mils**
> **50 mil** probes center to center spacing requirement: **50 mils**
> **39 mils** probe center to center spacing requirement: **39 mils**

8. Ground Test points selection

Number of required Ground test points can be estimated as **10%** of connected nodes. The ground test points should be distributed evenly across the board.

9. Component edge to Test Point Spacing Clearance

Guided/Non-Guided	Component Height	Component Edge to test point center spacing
Non- Guided	< .060”	.038”
Non- Guided	.060” < comp. Height < .100”	.038”
Non- Guided	.100” < comp. Height < .300”	.053”
Non- Guided	> .300”	.116”
Guided	< .060”	.038”
Guided	.060” < comp. Height < .100”	.094”
Guided	.100” < comp. Height < .300”	.094”
Guided	> .300”	.124”

10. Test target priorities

Test target priorities in order of preference:
1- Test Pads, 2- Vias, 3- Component leads

Device pins (through-hole), test pads, connectors, and vias can be used to allow adequate test access. For PCBs using Surface Mount Technology (SMT), test pads must be used since probing may damage the leads and open solder connections may be temporarily connected when the probe presses the leads onto the trace surface.
Where via probing is necessary, soldering or gold plating the vias provides a good probing surface. Vias must not be solder masked as this will insulate and block probe contact.